



Features

- Single 3-V Supply Voltage
- High Power-added Efficient Power Amplifier (P_{out} typically 26.5 dBm)
- Ramp-controlled Output Power
- Low-noise Preamplifier (NF typically 1.8 dB)
- Biasing for External PIN Diode T/R Switch
- Current-saving Standby Mode
- Few External Components

Electrostatic sensitive device.
Observe precautions for handling.



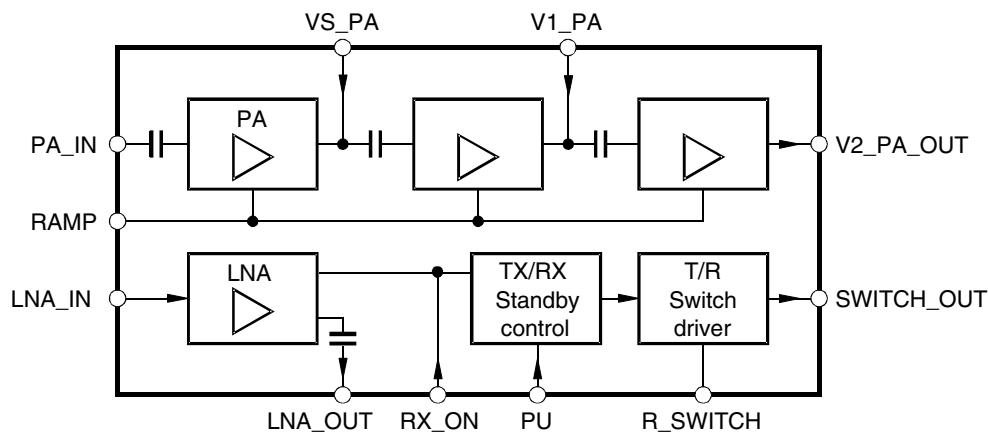
DECT SiGe Front End IC

U7004B

Description

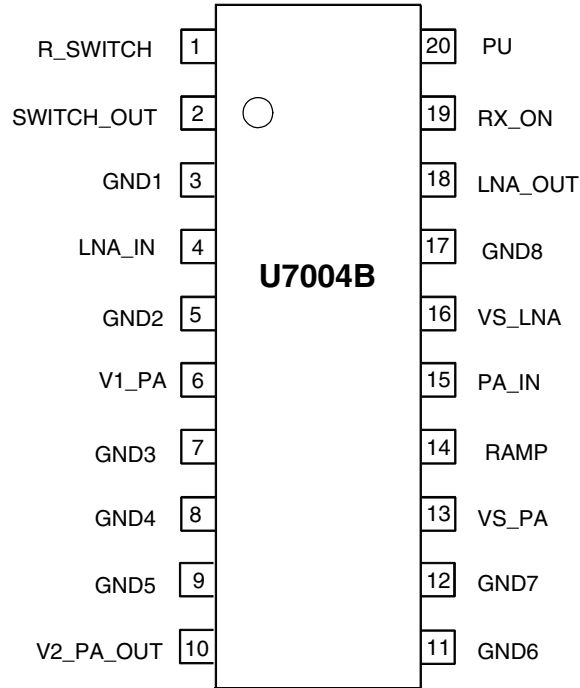
The U7004B is a monolithic SiGe transmit/receive front end IC with power amplifier, 50- Ω internal matching, low-noise amplifier and T/R switch driver. It is especially designed for operation in TDMA systems like DECT. Due to the ramp-control feature and a very low quiescent current, an external switch transistor for V_S is not required.

Figure 1. Block Diagram



Pin Configuration

Figure 2. Pinning SSO20



Pin Description

Pin	Symbol	Function
1	R_SWITCH	Resistor to GND sets the PIN diode current
2	SWITCH_OUT	Switched current output for PIN diode
3	GND1	Ground
4	LNA_IN	Low-noise amplifier input
5	GND2	Ground
6	V1_PA	Inductor to power supply for power amplifier
7	GND3	Ground
8	GND4	Ground
9	GND5	Ground
10	V2_PA_OUT	Inductor to power supply and matching network for power amplifier output
11	GND6	Ground
12	GND7	Ground
13	VS_PA	Supply voltage for power amplifier
14	RAMP	Power-ramping control input
15	PA_IN	Power amplifier input
16	VS_LNA	Supply-voltage input for low-noise amplifier
17	GND8	Ground
18	LNA_OUT	Low-noise amplifier output
19	RX_ON	RX active high
20	PU	Power-up active high

Absolute Maximum Ratings

All voltages refer to GND (pins 3, 5, 7, 8, 9, 11, 12 and 17), ESD protection according to ESD-S5.2-1994, Class M1.

Parameters	Symbol	Value	Unit
Supply voltage pins 6, 10, 13 and 16 (no RF)	V_S	5	V
Duty cycle PA		50	%
Burst duration PA		5	ms
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	-40 to +125	°C
Input power PA pin 15	P_{inPA}	+10	dBm
Input power LNA pin 4	P_{inLNA}	-5	dBm

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	95	K/W

Operating Range

All voltages refer to GND (Pins 3, 5, 7, 8, 9, 11, 12 and 17). The following table represents the sum of all supply currents depending on the TX/RX mode. Power supply points are VS_LNA, VS_PA, V1_PA, V2_PA_OUT.

Parameters	Symbol	Min.	Typ.	Max.	Unit
Supply voltage pins 6, 10 and 13	V_S	2.7	3.6	4.6	V
Supply voltage pin 16	V_S	2.7	3.6	4.6	V
Supply current TX	I_S		450		mA
RX	I_S		8		mA
Standby current PU = 0	I_S		10		μA
Ambient temperature	T_{amb}	-25	+25	+70	°C

Electrical Characteristics

Test conditions (unless otherwise specified): $V_S = 3.6$ V, $T_{amb} = 25^\circ\text{C}$, pulsed mode, duty cycle 4.17%, $t_{on} = 417$ μs

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Power Amplifier ⁽¹⁾						
Supply voltage	Pins 6, 10 and 13	V_S	2.7	3.6	4.6	V
Supply current	TX	I_{S_TX}		450		mA
Supply current	RX (PA off)	I_{S_RX}			10	μA
Standby current	Standby	$I_{S_standby}$			10	μA
Frequency range	TX	f	1.88		1.94	GHz
Power gain	TX, pin 15 to pin 10	Gp		28		dB
Gain-control range	TX	ΔGp		48		dB

- Notes:
1. Power amplifier shall be unconditionally stable, maximum duty cycle 50%, maximum load mismatch and duration: load VSWR = 20:1 (all phases) 10 s, $Z_G = 50 \Omega$
 2. With external matching network (see Figure 13 and Figure 14)
 3. Low-noise amplifier shall be unconditionally stable

Electrical Characteristics (Continued)

Test conditions (unless otherwise specified): $V_S = 3.6\text{ V}$, $T_{\text{amb}} = 25^\circ\text{C}$, pulsed mode, duty cycle 4.17%, $t_{\text{on}} = 417\text{ }\mu\text{s}$

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Ramping voltage	TX, power gain (max), pin 14	$V_{\text{RAMP max}}$		2.1		V
Ramping current	TX, power gain (max), pin 14	I_{RAMP}		0.5	2.0	mA
Power-added efficiency	TX	PAE		30		%
Saturated output power	TX, refer to pin 10	P_{sat}		26.5		dBm
Input matching ⁽²⁾	TX, pin 15	VSWRin		< 2:1		
Output matching ⁽²⁾	TX, pin 10	VSWRout		< 2:1		
Harmonics at P 1dB	TX, pin 10	2 fo 3 fo		-30		dBc
Maximum input power	Pin 15	P_{inPA}		10		dBm
Stability (non harmonic emission)	TX, pin 10 $P_{\text{in}} = 2\text{ dBm}$, $V_{\text{RAMP}} = 2\text{ V}$ VSWRout < 10:1 (all phases)			-60		dBc
T/R Switch Driver (Currently Programmed by External Resistor from R_SWITCH to GND)						
Switch-out current output	Standby, pin 2	$I_{\text{S_O standby}}$			2	μA
Switch-out current output	RX	$I_{\text{S_O RX}}$			2	μA
Switch-out current output	TX at 100 Ω	$I_{\text{S_O 100}}$		1		mA
Switch-out current output	TX at 1.2 k Ω	$I_{\text{S_O 1k2}}$		3		mA
Switch-out current output	TX at 33 k Ω	$I_{\text{S_O 33k}}$		10		mA
Low-noise Amplifier ⁽³⁾						
Supply voltage	All, pin 16	V_S	2.7	3.6	4.6	V
Supply current	RX	I_S		8		mA
Supply current (LNA and control logic)	TX (control logic active), pin 16	I_S		300		μA
Standby current	Standby, pin 16	I_S		1	10	μA
Frequency range	RX	f	1.88		1.94	GHz
Power gain	RX, pin 4 to pin 18	Gp	17	19		dB
Noise figure	RX	NF		1.8	2.0	dB
Gain compression	RX, refer to pin 18	P1dB		-7		dBm
3rd-order input interception point	RX	IIP3		-15		dBm
Input matching	RX	VSWRin		< 2:1		
Output matching	RX	VSWRin		< 2:1		
Logic Input Levels (RX_ON, PU)						
High input level	= 1, pins 19 and 20	V_{IH}	2.4		V_S	V
Low input level	= 0	V_{IL}	0		0.5	V
High input current	= 1	I_{IH}		40		μA
Low input current	= 0	I_{IL}		0		μA

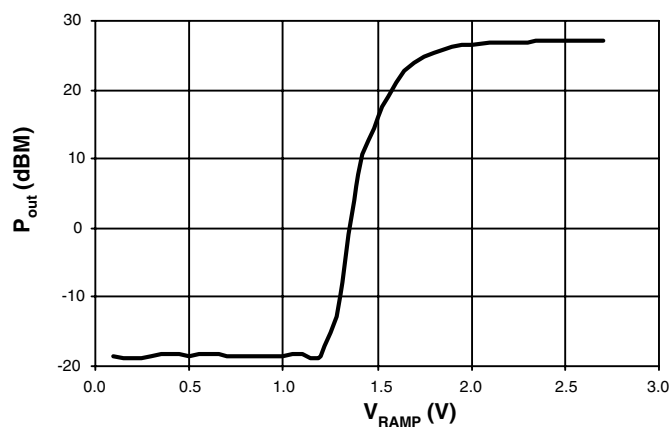
- Notes:
1. Power amplifier shall be unconditionally stable, maximum duty cycle 50%, maximum load mismatch and duration: load VSWR = 20:1 (all phases) 10 s, $Z_G = 50\text{ }\Omega$
 2. With external matching network (see Figure 13 and Figure 14)
 3. Low-noise amplifier shall be unconditionally stable

Control Logic

Table 1. Control Logic for LNA and T/R Switch Driver

Operation Mode	PU	RX_ON
Standby	0	0
TX	1	0
RX	1	1

Figure 3. Output Power versus Ramp Voltage



Input/Output Circuits

Figure 4. Input Circuit PA_IN/VS_PA

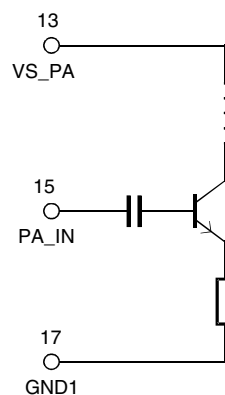


Figure 5. Input Circuit RAMP/VS_PA

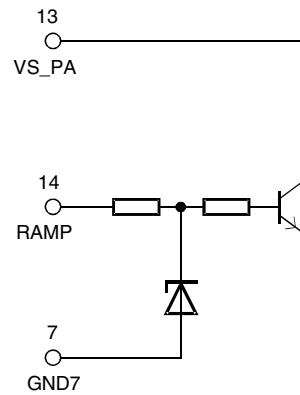


Figure 6. Input Circuit V1_PA

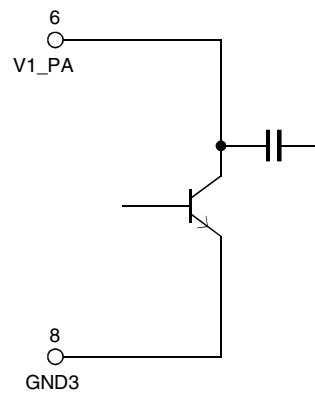


Figure 7. Input/Output Circuit V2_PA

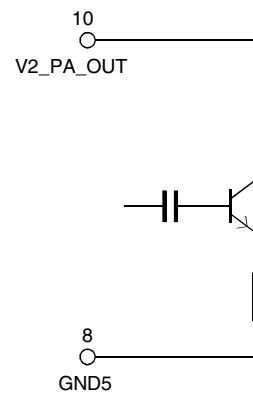


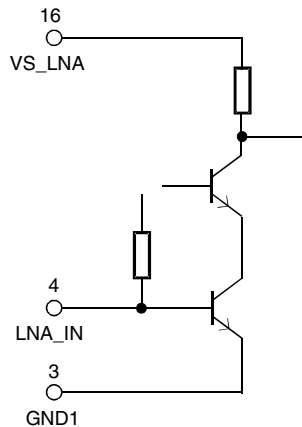
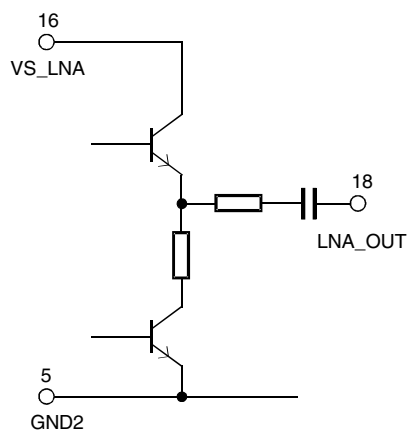
Figure 8. Input Circuit LNA_IN/VS_LNA**Figure 9.** Output Circuit LNA_OUT

Figure 10. Input Circuit SWITCH_OUT/R_SWITCH

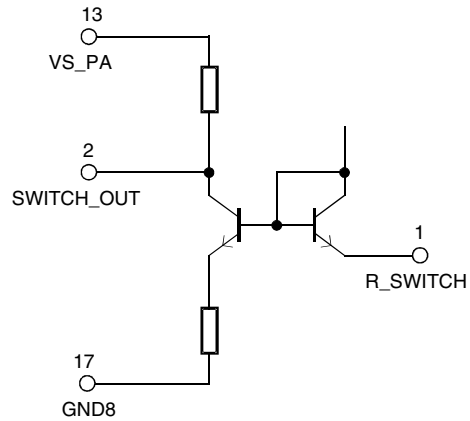


Figure 11. Input Circuit RX_ON

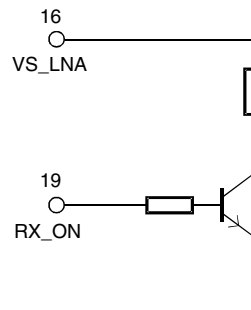
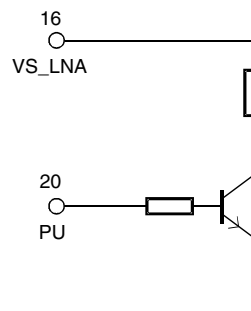
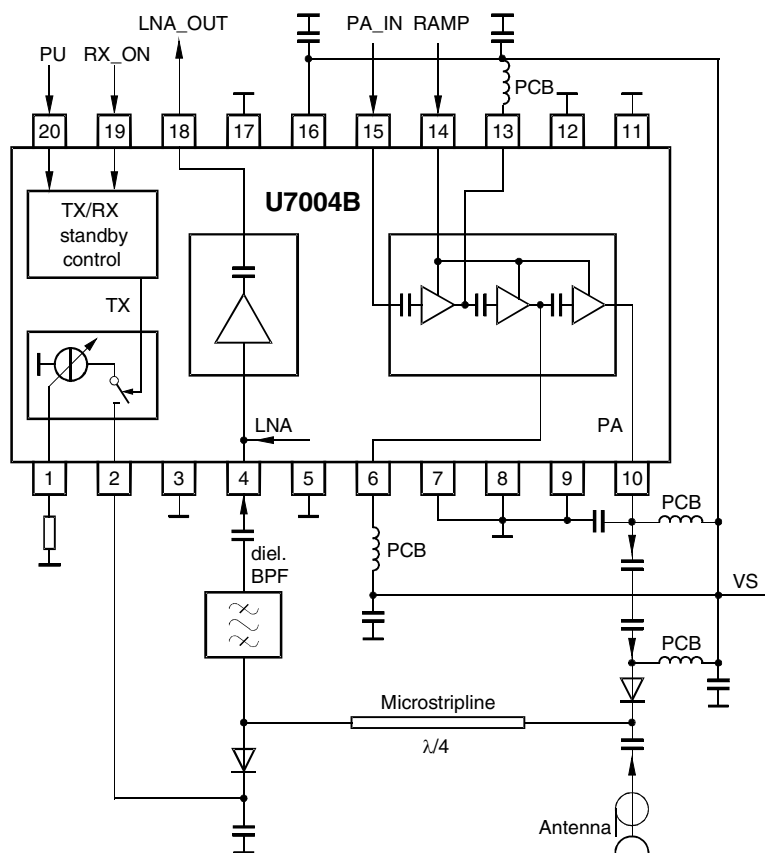


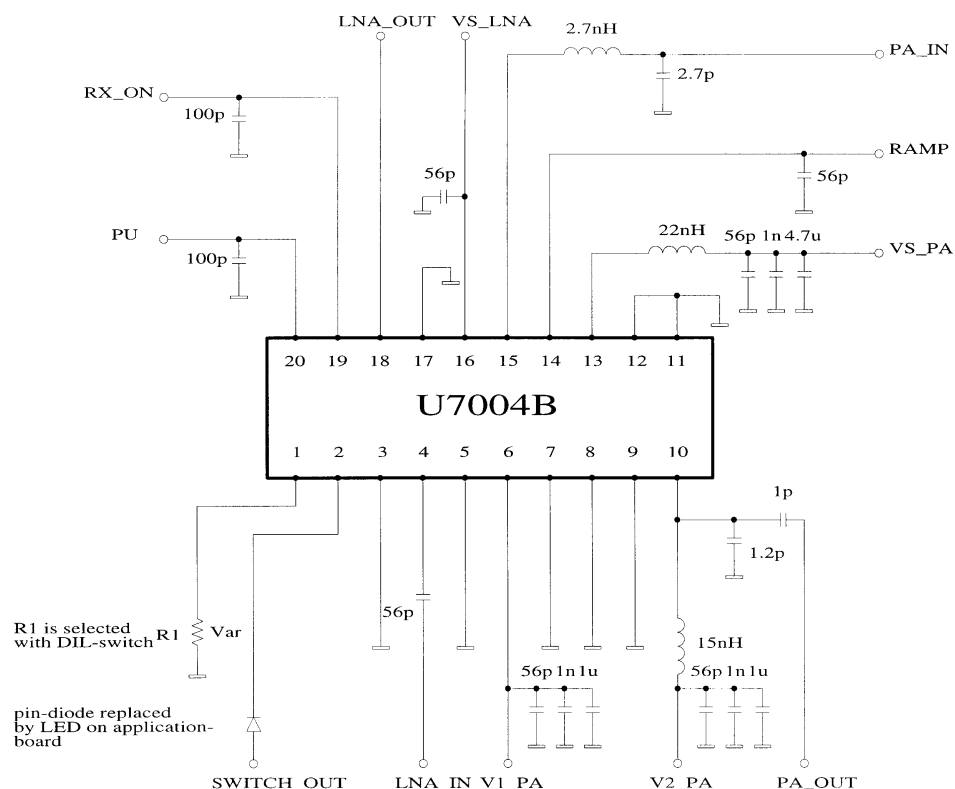
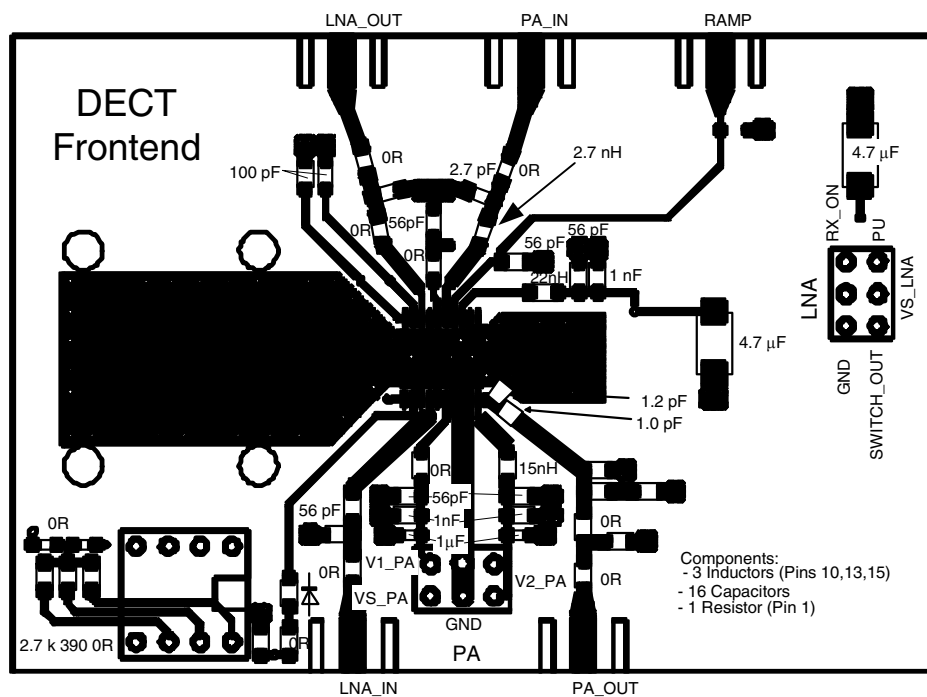
Figure 12. Input Circuit PU



Typical Application Circuit

Figure 13. Typical Schematic





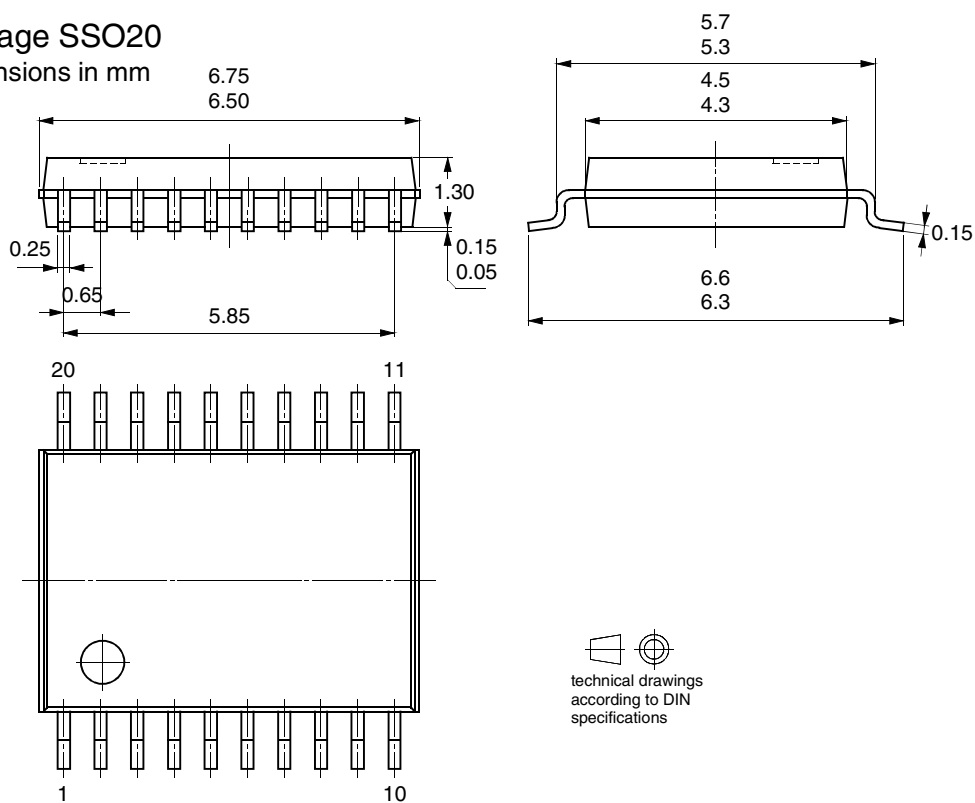
Ordering Information

Extended Type Number	Package	Remarks
U7004B-MFS	SSO20	Tube
U7004B-MFSG3	SSO20	Taped and reeled

Package Information

Package SSO20

Dimensions in mm





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